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# INFORMATION DISCLOSURE STATEMENT BY APPLICANT

*(Multiple sheets used when necessary)*

SHEET 1 OF 4

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| Application No. | 10/800,390 |
| Filing Date | 12 March 2004 |
| First Named Inventor | Paul D. Brabant |
| Art Unit | 2818 |
| Examiner | David Vu |
| Attorney Docket No. | ASMEX.448A |

**U.S. PATENT DOCUMENTS**

| Examiner Initials | Cite No. | Document Number *Number - Kind Code (if known)* Example: 1,234,567 B1 | Publication Date MM-DD-YYYY | Name of Patentee or Applicant | Pages, Columns, Lines Where Relevant Passages or Relevant Figures Appear |
|---|---|---|---|---|---|
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| | 5 | 6,373,112 | 04/16/02 | Murthy et al. | |
| | 6 | 6,537,370 | 03/25/03 | Hernandez et al. | |
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| | 8 | 2002/0173130 | 11/21/02 | Pomerede et al. | |
| | 9 | 2003/0190791 | 10/09/03 | Fischetti, et al. | |
| | 10 | 2003/0235931 | 12/25/03 | Wada et al. | |
| DV | 11 | 2004/0219735 | 11/04/04 | Brabant et al. | |

**FOREIGN PATENT DOCUMENTS**

| Examiner Initials | Cite No. | Foreign Patent Document *Country Code-Number-Kind Code* Example: JP 1234567 A1 | Publication Date MM-DD-YYYY | Name of Patentee or Applicant | Pages, Columns, Lines Where Relevant Passages or Relevant Figures Appear | T[1] |
|---|---|---|---|---|---|---|
| DV | 12 | WO 01/41544 | 06/14/01 | PCT | | |

**NON PATENT LITERATURE DOCUMENTS**

| Examiner Initials | Cite No. | Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published. | T[1] |
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| DV | 13 | BAUER et al., "Relaxed SiGe buffers with thicknesses below 0.1 μm", *Thin Solid Films* 369:152–156 (2000). | |
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| Examiner Signature | Date Considered 01/21/06 |
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| DV | 25 | KASPER, "Prospects of SiGe Heterodevices", *Journal of Crystal Growth* 150:921–925 (1995). | |
| DV | 26 | KASPER et al., "New virtual substrate concept for vertical MOS transistors", *Thin Solid Films* 336:319–322 (1998). | |

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| DV | 27 | LEE et al., "Strained Ge channel p-type metal–oxide–semiconductor field-effect transistors grown on $Si_{1-x}Ge_x$/Si virtual substrates", *Applied Physics Letters* 79:3344–3346 (2001). | |
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| DV | 36 | REINKING et al., "Ge p-MOSFETs compatible with Si CMOS-technology", *Proceedings of the 29th ESSDERC* 99:300–303 (1999). | |
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| DV | 38 | SCHÖLLHORN et al., "Coalescence of germanium islands on silicon", *Thin Solid Films* 336:109–111 (1998). | |
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